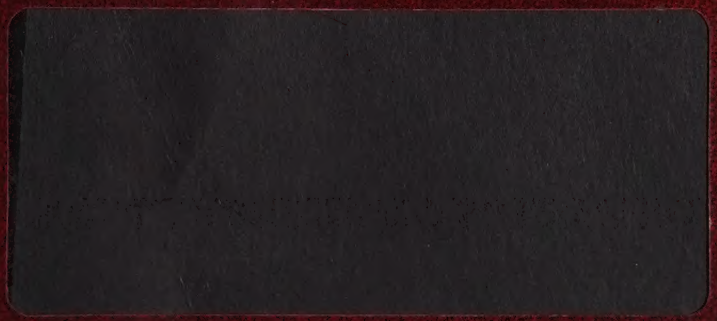
Instruction manual



DATA I/O

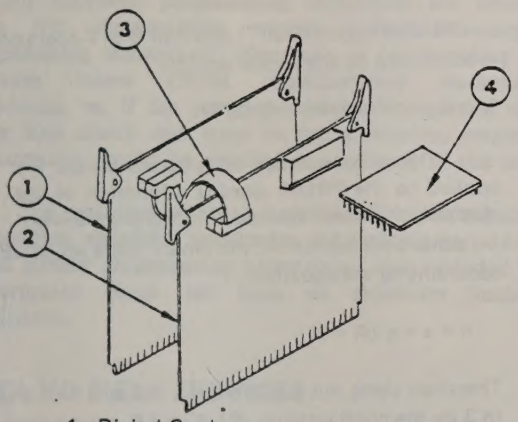
Programming systems for tomorrow...today

PROM PROGRAMMER
Program Card Set

025-1416-1 909-1416-1

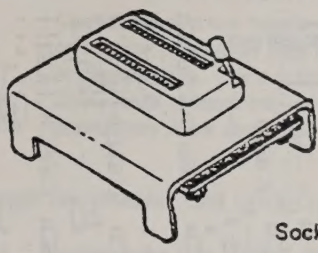
REV E JAN. 79

SPECIFICATION



1. Digital Card	701-1446
2. Analog Card	701-1416-1
3. Interconnect Cable	709-1608
4. Calib. Program Adapter	910-1416-1

Figure 1-1. Program Card Set 909-1416-1.



Socket Adapter

Table 1-1. PROM types to Data I/O Socket Adapters.

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
INTERSIL				
512X8 MOS	6604	VOL TS	24 PIN	1450
1024X4 MOS	6603	VOL TS	24 PIN	1449

DESCRIPTION

Program (Personality) Card Set 909-1416-1, with the appropriate Socket Adapter, provides Data I/O PROM programmers with the capability of programming and reading the PROMs listed in Table 1-1. Socket Adapters are available for each PROM listed. Table 1-1 references the Socket Adapters required to program (or read) the various PROMs.

INSTALLATION

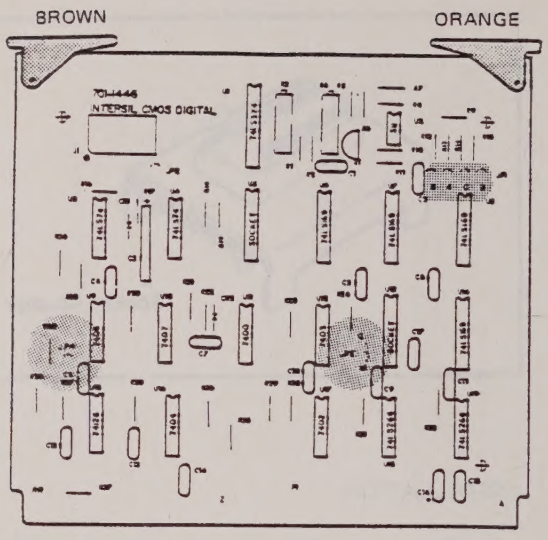
Turn power OFF while changing Card Sets. Install the Digital Card in programmer Brown-Orange card slot; install the interconnected Analog Card in White-White card slot. Component sides of cards should face forward in programmer Models 1-5, to the right in programmer satellites, and down in programmer Models 7 and 9. Connect J2 on Analog Card to front panel Socket Receptacle. Refer to the programmer manual for more detailed installation instructions.

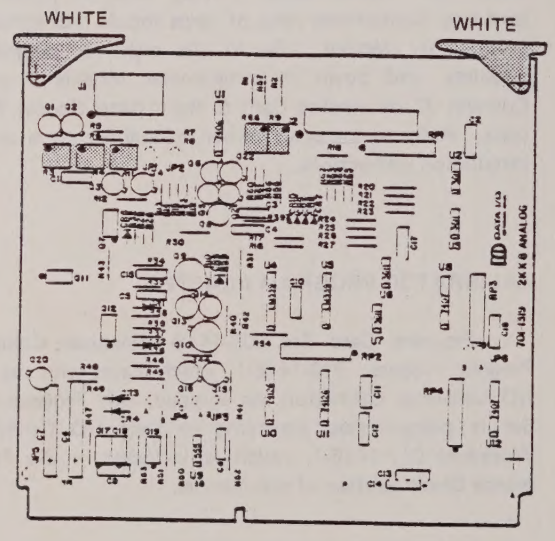
CALIBRATOR PROGRAM ADAPTER

Program Card Set 909-1416-1 includes Calibrator Program Adapter 910-1416-1, which mates with the Data I/O Universal Calibrator. As shipped, this Program Card Set is precalibrated according to Data I/O Calibration Procedure 017-1416-1, which is included in the Performance Check Section of this manual.

CALIBRATION AND PERFORMANCE CHECK

Card Set calibration and performance verification procedures are given in the following pages. Calibration should be performed every 90 days, or if PROM programming yields fall below PROM manufacturers' recommendations. Performance Check should be performed after each calibration.





DIGITAL JUMPERS

4/8 BIT (JP4)

JP4 is left open (8 BIT) and 4 or 8 BIT operation is controlled by the socket adapter.

Intelligent Programming (JP1)

The total number of program pulses (n) applied to the PROM word is a function of the number of pulses required to program the word (x) times a multiplier (A, the binary value set by JP1) according to the equation:

$$n = x + x (A + 1)$$

Therefore using this equation, if x is 5 and "A" is set to 3 by the configuration JP1 A and B, then a total of 5 + 5 (3 + 1) or 25 pulses would be applied.

Reject Limit (JP 3)

The reject jumper is set to C.

If a word has not programmed after 8 program pulses, Reject is signaled. On the Model 5, the verify A and B lights extinguish, and the program and interrupt lights stay on. On Models 7 and 9, the execute light extinguishes, and the P indicator flashes.

ANALOG ADJUSTMENT LOCATIONS

Analog adjustment locations are shown shaded.

CALIBRATION/PERFORMANCE CHECK

INTRODUCTION

Since PROM manufacturers' shipments can vary from lot to lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers employ manufacturer-approved programming techniques: therefore, if programming yields diminish below PROM manufacturers' recommended minimums, or, if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked as explained in this section.

The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

DATA I/O FIELD SERVICES

Data I/O, Corp. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

TEST EQUIPMENT REQUIRED

To perform a complete performance check, the following equipment is required:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Prog. 1, 2, 3, 5: Data I/O Extender Card, P/N 910-1136.
   B. Prog. 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A, or equivalent

4. Adjustment Tool: A three-inch screwdriver

5. Dual Trace Oscilloscope: Tektronix 465, or equivalent

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-2608.

8. Jumper wires approximately 12 inches in length.

INSTALLATION OF UNIVERSAL CALIBRATOR

The following installation procedure assumes that the Universal Calibrator is mated with the Extender Card and that programmer power is off. On Programmers 1, 2, 3, and 5, remove the top cover to expose the card cage. To expose the card cage on the Model 9, open the access opening on the front of the chassis.

1. Remove end of 26-conductor cable from analog card. Remove both cards (analog and digital) from Programmer (or Satellite) card cage.

2. Remove end of 16 conductor cable from digital card J1.

CAUTION

Connector pins are fragile; careless connector extraction may result in bent or broken pins. Use a suitable tool—like a small screwdriver—when removing connectors from their sockets.

3. Install the extender card (with the Universal Calibrator in place).
   A. Programmers 1-5: Install the extender card into the analog card slot (white-white).
   B. Programmer 9: Install extender fixture into digital card slot (brown- orange).

4. A. Programmers 1-5: Install the analog card of the program card set into the card slot on top of the extender board. Refer to Figure 1.
   B. Programmer Model 9: Install the analog card in front card slot. Refer to Figure 2. The components should face the Calibrator.

5. A. Programmers 1-5: Install the digital card in the digital slot in the programmer.
   B. Programmer 9: Install the digital card behind the analog card on top of the extender card.

6. Making sure that cable red stripes and connector pins 1 are properly oriented, connect the analog card to the Universal Calibrator as follows:
   A. Programmers 1-5: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Connect J2 of the analog card to J2 of the Universal Calibrator using the ribbon cable that connects the card set and the programmer.
   B. Programmer 9: Connect J1 of the analog card to J1 of the Universal Calibrator using the strap between the analog and digital cards. Using the 26-connector cable supplied with the Calibrator, connect J2 of the analog card to J2 of the Calibrator.

7. Plug Calibrator Program Adapter into PROGRAM ADAPTER SOCKET on Universal Calibrator.

CAUTION

Be sure that the four-digit portions of both part numbers are identical: i.e. Analog card 701-XXXX is part of program card set 909-XXXX, which is calibrated by calibrator program adapter 910-XXXX.

8. Connect DVM ground probe to GND test point at left side of Universal Calibrator.

This completes installation of the Universal Calibrator.

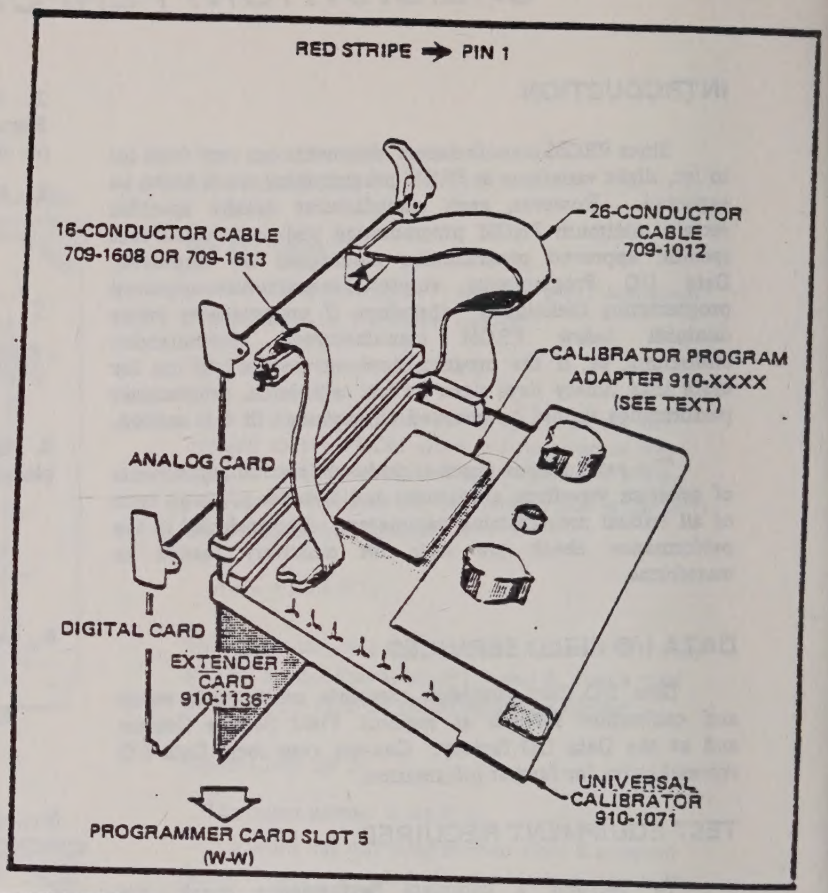


Figure 1. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for Calibration/Performance Check.

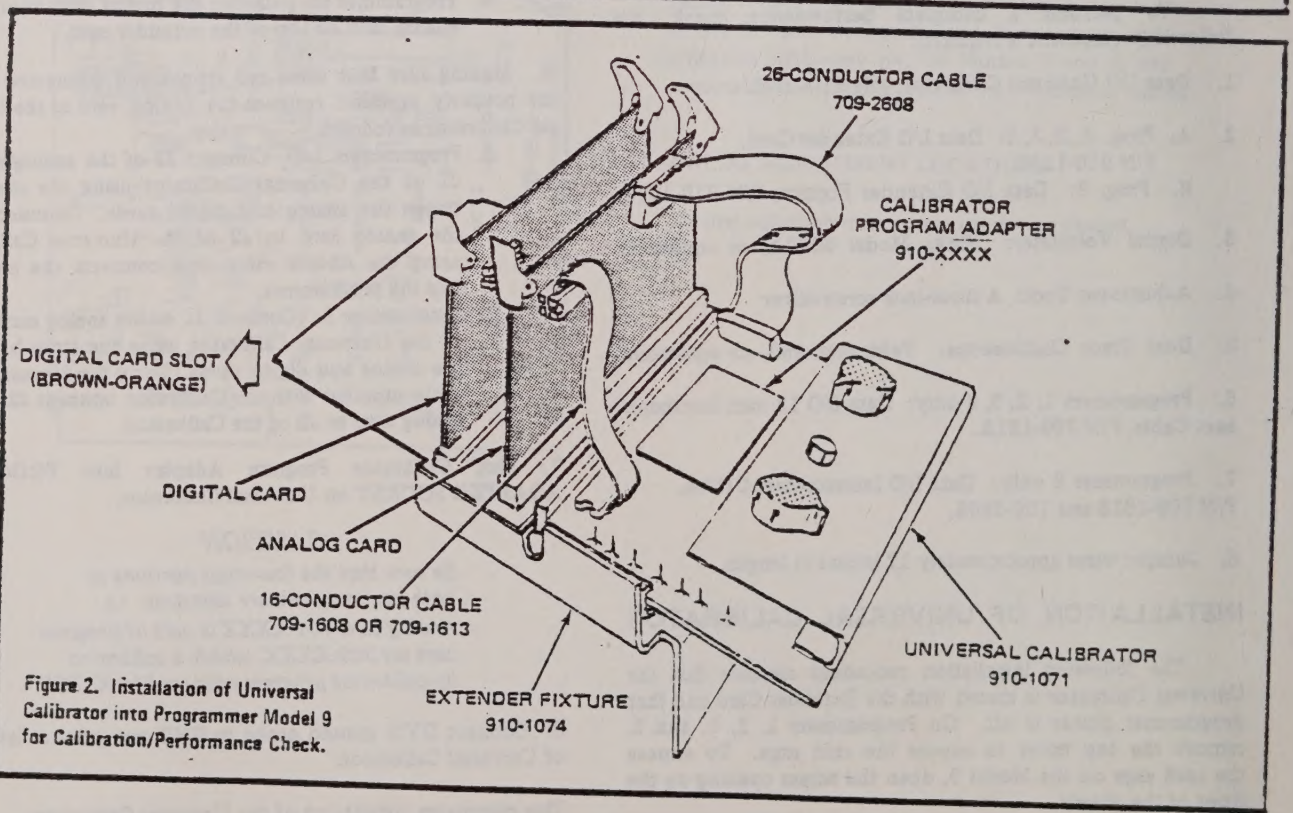


Figure 2. Installation of Universal Calibrator into Programmer Model 9 for Calibration/Performance Check.

CALIBRATION CHART

The calibration chart is to be used only with the (calibrator) program adapter specified in the title block of the chart.

The left-most portion of the chart contains truth tables for the calibrator program adapter. The truth tables are for documentation purposes only, and have no bearing on the actual performance check/calibration procedures.

PROGRAMMER WORD COUNT COLUMN is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When using the chart, refer to the address (word count) corresponding to the address readout configuration of the programmer in use. For instance, if your programmer has a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to compo-components if Programmer is left unattended with advanced word count.

TEST DESCRIPTION column contains three kinds of tests: (1) power supplies, (2) performance checks, and (3) calibration adjustments. The power supply tests are contained in the first five rows of the chart. (Note that power supply adjustments are located in the programmer, not in the program card set.) Performance checks fill the bulk of the Calibration Chart; these are characterized by min/max voltage limits only. No nominal (NOM) values are given, and no adjustments (ADJ) are prescribed.

Calibration steps are those with entries in the ADJ and NOM columns. These steps are evident by the note "CALIBRATION STEP" in the comments column.

SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load select switch; S3 is the line select switch. Generally, each step on the Calibration Chart requires changing of switch positions. S1 is push to test, and should be held depressed only long enough to obtain a DVM reading.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high Programmer current levels. Extended high current operation (S1 depressed) may damage sensitive electronic components.

TEST POINT column gives test point location for DVM probe on Universal Calibrator. Some test points are located on the program card itself; for instance, if a test point is designated as U6 P8, it means that the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the comments column.

The ADJ column calls out potientiometer designations. The first four entries in the ADJ column refer to power supply potientiometers located on the power supply board of the Programmer. If adjustments are required, refer to Programmer manual. The remaining entries in the ADJ column refer to pots on the analog card. These are located as shown on page 1-2 in the Specifications section of this manual.

The LIMITS COLUMN is divided into three portions: MIN (minimum), NOM (Nominal), and MAX (Maximum). The values given are in volts, and indicate the range into which a given DVM reading should fall when S1 is pressed. If a reading is within the limits, no adjustment is required and the programmer (or program card set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (calibration steps), the card is non functional and should not be used for programming.

NOTES are written in a block at the bottom of the calibration chart. These apply to certain calibration steps and are referenced by numbers in the comments column. Notes called out by letter in the comments column apply only to Model IX calibration.

PERFORMANCE CHECK AND CALIBRATION PROCEDURE

DC CALIBRATION

The following paragraphs describe the method by which a program card set is checked/calibrated in conjunction with the applicable Calibration Chart. The procedure assumes that the Universal Calibrator is properly installed, as previously described. The following procedure should be performed with the programmer in an ambient temperature range between 15°C to 35°C.

Initialization

1. Switch Programmer power ON; allow Programmer to warm up for approximately five minutes.
2. Programmers 1, 2, 3, and 5:
   Press: RESET
   ROM2-ROM2
   MANUAL
   PROGRAM
   START

   Programmer 9:
   Press: EXECUTE
   Set NORMAL/INVERT switch to INVERT.

Power Supply

During the procedure the programmer card cage should contain all boards normally used.

Connect DVM between GND and the Universal Calibrator test points given in Steps 1-1 through 1-5 on the Calibration Chart. Measured voltages should fall within the given limits. (Calibrator Switch positions do not matter.)

If any power supply voltage measurement reading is outside of the given range, adjustment must be made. Power supply adjustments are located on the power supply board within the Programmer.

If a Programmer Satellite is being used, check/calibrate Satellite power supply as explained in Satellite Manual.

Performance Check/Calibration

1. Use FWD and REV keys on Programmer keyboard to index the "address display" (word count) to the decimal (DEC), hexadecimal (HEX), or octal (OCT) address given in the word count column of the calibration chart.

CAUTION

DO NOT leave Word Count advanced beyond 000 for extended periods. Static (DC steady state) conditions created by the Universal Calibrator may cause thermal damage to components if Programmer is left unattended with advanced word count. Press Reset to relieve possible thermal stresses.

2. With Word Count set, and DVM probes installed between GND and the indicated test point on the universal calibrator, set switches S2 and S3 to the positions indicated. Press S1 to test.

CAUTION

DO NOT hold S1 depressed for extended periods. Certain measurements induce high current levels within the Programmer. Extended high current operation (S1 depressed) puts unnecessary stress on sensitive electronic components.

3. While S1 is held, DVM readings should fall between the indicated limits for each measurement. If a DVM reading is outside of limits, or if the reading cannot be adjusted to fall within limits (ADJ column), DO NOT use the card set for programming.

Proceed through the Calibration Chart until all tests have been performed. At the conclusion of testing, turn Programmer power OFF, and proceed to AC Dynamic Tests.

AC CALIBRATION

AC Dynamic Tests

The following procedure is used to obtain the "Program Waveforms" shown on the Timing Diagram at the rear of this manual.

These waveforms, indicated by circled digits (①,②,③,..) on the timing diagram, are identically referenced on the Calibration Chart. The waveforms are obtained by selecting switch positions (S2 and S3) on the Universal Calibrator and feeding the selected signals to an appropriately triggered dual trace oscilloscope.

Test Set-Up

1. Make sure that programmer power is Off.

2. A. Programmers 1-5: Remove the digital card from the card cage. Refer to Figure 3.
   B. Programmer 9: Remove the digital card from the extender. Refer to Figure 4.

3. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

4. A. Programmers 1-5: Disconnect the other end of the 16-conductor cable from J1 of the analog card. Substitute the 13 inch cable supplied with the Calibrator, and connect J1 of the analog card to J1 of the digital card.
   B. Programmer 9: Connect the free end of the 16-conductor cable to digital card J1, assuring that cable red stripe and connector pin 1 are properly oriented.

5. Connect triggered input channel of dual trace oscilloscope to digital card test pulse. The location of the test pulse on the digital card is noted to the left of the Test waveform on the timing diagram. Connect the other channel to TP3 on the Calibrator. Re-install the digital card per step 2, above.

6. Using a suitable jumper cable, connect the Read Enable line emanating from analog card J1-16 to ground. (Use either the programmer chassis or the GND test point on the Universal Calibrator.)

7. Programmer 9: Set NORMAL/INVERT switch to INVERT.

CAUTION

Make sure that J1-16 is properly connected to ground. If it is inadvertently connected to any other potential, damage to Programmer components may result.

8. Turn Programmer power ON.

9. Programmers 1, 2, 3, 5:
   Press: RESET
   RAM-RAM
   PROGRAM
   MANUAL
   START
   Programmer 9:
   Press: KEYBOARD

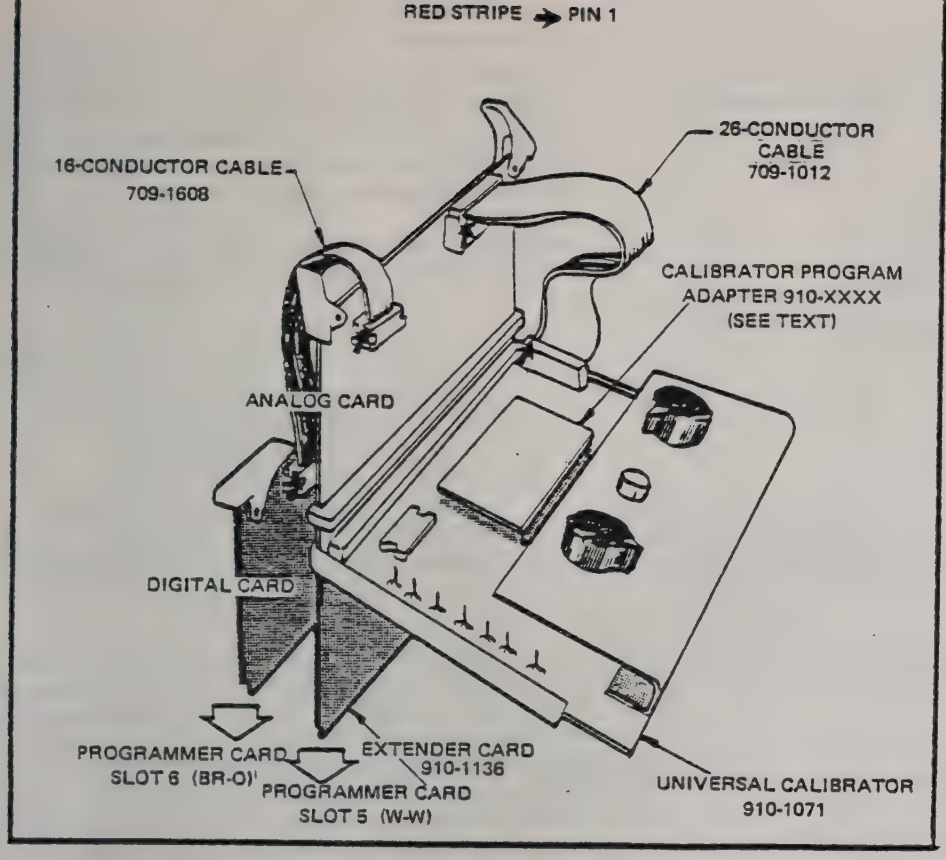


Figure 3. Installation of Universal Calibrator into Programmer Models 1, 2, 3, and 5 for AC Dynamic Tests.

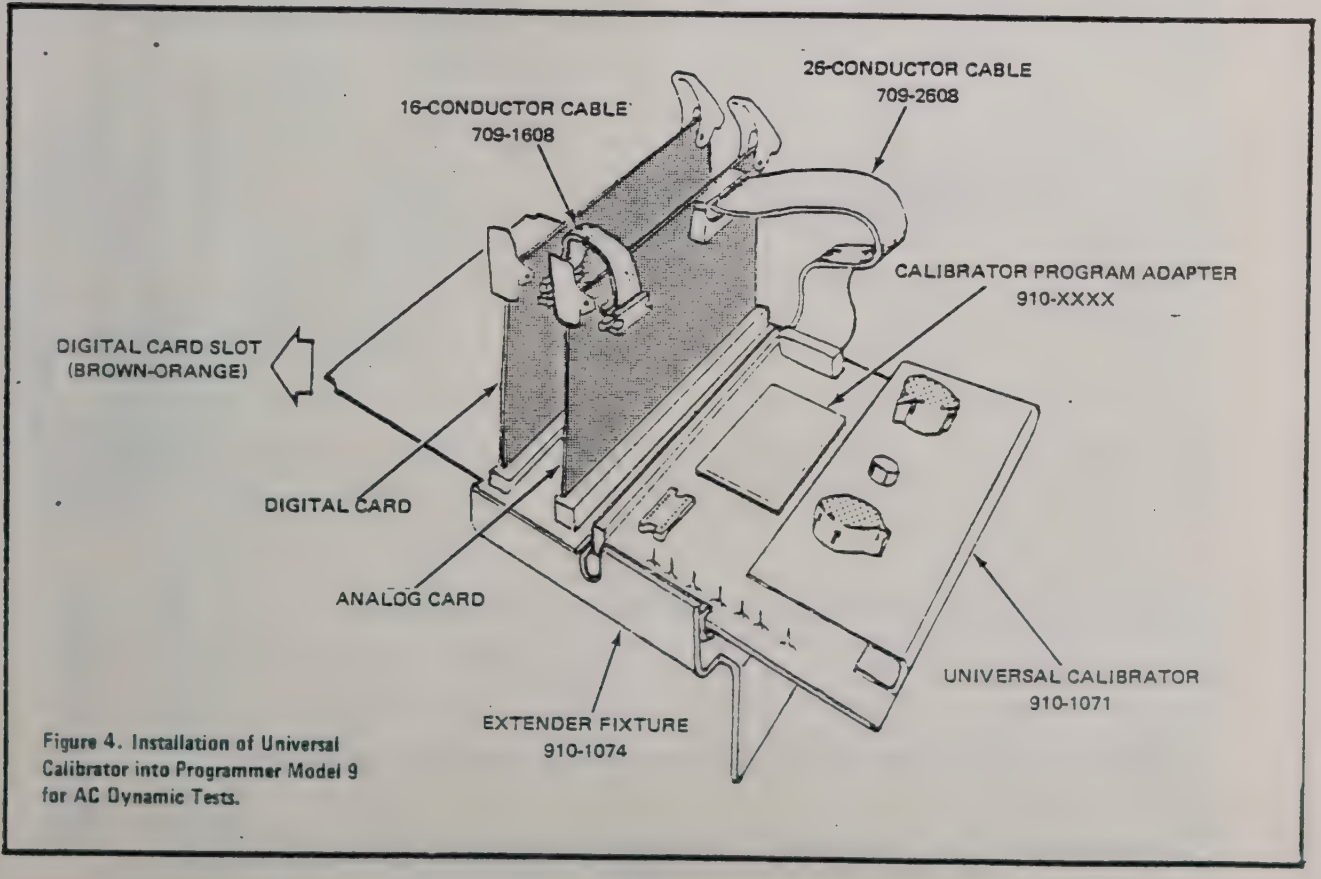


Figure 4. Installation of Universal Calibrator into Programmer Model 9 for AC Dynamic Tests.

10. Load approximately ten RAM addresses with bit 1 (only). This is accomplished by pressing 1 and FWD repetitively, or a tape may be used.

11. Programmers 1, 2, 3, 5:

Press: RESET
PROG
AUTO
RAM-ROM2

Programmer 9:

Press: PROGRAM

Waveform Observations

Initiate waveforms:

Programmers 1-5: press START.
Programmer 9: press EXECUTE.

The machine will stop on those addresses loaded in step 10 of the test set-up. If an abort condition is indicated, press WORD SKIP (SKIP on the Model 9) to advance the word count and repeat output of programming waveforms. An abort condition is indicated on Models 1, 2, 3, and 5 if the PROGRAMMING and INTERRUPT indicators come on. A Model 9 displays an abort condition by flashing the "P" indicator.

The "Program Waveforms" on the timing diagram at the rear of the manual are cross-referenced to the "Test Description" column on the Calibration Chart by circled digits (①, ②, ③ ,...). To obtain the various waveforms use S2 and S3 on the Universal Calibrator to select the positions indicated in the "Switch Positions" column of the calibration chart and press S1 to test. S3 routes analog card output to TP3 (oscilloscope probe); S2 selects resistive loads, which are connected to ground when S1 is pressed.

NOTE: *All other information on the calibration charts is of no importance during waveform observations.*

CAUTION

When S1 is pressed high currents are induced within the Programmer; do not hold S1 depressed for extended periods. High currents are also present when the programmer is locked into program mode with advanced word count; RESET before leaving programmer unattended during these tests.

During these tests note that the Abort, Pause, and Reject functions of the program card set remain active; Press WORD SKIP to refresh the display. The abort timer signals a reject after a specific programming time. The pause timer controls the on/off time of the programming function. The position of the reject jumper (C or M) limits the number of applied programming pulses. Refer to the notes column of the timing diagram for definitions of the abort, pause, and reject functions.

DATA I/O
REDMOND, WASH.

CALIBRATION CHART 017-1416-1
FIXTURE 702-1071
PROGRAM ADAPTER 910-1416-1
PROGRAM CARD 909-1416-1

MANUFACTURE INTERSIL
PROM 1M6603/04

DATE	SYM	REVISION RECORD	DR	CK
12-8[illegible]		ECN #2603	KL	SC
12-8	-	ECN #2565	FS	SC
1-79	E	ECN #2749	KL	[illegible]

PROM U5 J1 16 15 14 13 12 11 10 — PROM U4 J1 9 8 7 6 5 4 3 2 1 J1

STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
1-1	000	00	000	+24			+24	R26	23.5	24.0	24.5
1-2	000	00	000	POWER +48			+48	R24	49.4	49.7	49.8
1-3	000	00	000	SUPPLY + 5			+ 5	R18	5.05	5.1	5.15
1-4	000	00	000	- 9			- 9	R40	-9.2	-9.0	-8.8
1-5	000	00	000	PROGRAMMABLE SUPPLY			+PROG		21.0	21.6	22.0
2-1	000	00	000	VCC ADJUST	5	1	TP3	R11	9.0	10.0	11.0
2-2	000	00	000	VCC CURRENT LIMIT	6	1	TP3		0.0		0.4
2-3	001	01	001	VCC READ (1)	5	1	TP3	R9	4.75	5.00	5.25
3-1	002	02	002	COMPARATOR REFERENCE			U5 P8		2.4		2.7
4-1	003	03	003	$\overline{CS}$ LEVEL (7)	7	5	TP3		0.0		0.4
4-2	004	04	004	$\overline{PE}$ PROGRAM (3)	7	6	TP3		-42.0	-44.0	-46.0
4-3	005	05	005	$\overline{PE}$ CURRENT LIMIT	6	6			0.0		0.4
4-4	006	06	006	PE VERIFY	4	6	TP3		3.7		4.7
4-5	007	07	007	STROBE HIGH (2)	7	7	TP3		4.5		5.5
4-6	008	08	010	STROBE LOW	7	7	TP3		0.0		0.4
5-1	009	09	011	BIT 8 PROGRAM	2	8	TP3		0.0		0.4
5-2	009	09	011	BIT 7 NO PROGRAM	2	9	TP3		2.2		2.8
5-3	009	09	011	BIT 6 PROGRAM	2	10	TP3		0.0		0.4
5-4	009	09	011	BIT 5 NO PROGRAM	2	11	TP3		2.2		2.8
5-5	009	09	011	BIT 4 PROGRAM	2	12	TP3		0.0		0.4
5-6	009	09	011	BIT 3 NO PROGRAM	2	23	TP3		2.2		2.8
5-7	009	09	011	BIT 2 PROGRAM	2	22	TP3		0.0		0.4
5-8	009	09	011	BIT 1 NO PROGRAM	2	21	TP3		2.2		2.8
5-9	009	09	011	BIT 8 NO PROGRAM	2	8	TP3		2.2		2.8
5-10	009	09	011	BIT 7 PROGRAM	2	9	TP3		0.0		0.4
5-11	009	09	011	BIT 6 NO PROGRAM	2	10	TP3		2.2		2.8
5-12	009	09	011	BIT 5 PROGRAM	2	11	TP3		0.0		0.4
5-13	009	09	011	BIT 4 NO PROGRAM	2	12	TP3		2.2		2.8
5-14	009	09	011	BIT 3 PROGRAM	2	23	TP3		0.0		0.4
5-15	009	09	011	BIT 2 NO PROGRAM (5)	2	22	TP3		2.2		2.8
5-16	009	09	011	BIT 1 PROGRAM (4)	2	21	TP3		0.0		0.4
5-17	010	0A	012	DATA DISABLE							
6-1	682	2AA	1252	ADDRESS TEST VIL (6)	7	20	TP3		0.0		0.4
6-2	682	2AA	1252	ADDRESS TEST VIH	3	19	TP3		1.3		1.9
6-3	682	2AA	1252	ADDRESS TEST VIL	3	18	TP3		0.0		0.4
6-4	682	2AA	1252	ADDRESS TEST VIH	3	17	TP3		1.3		1.9
6-5	682	2AA	1252	ADDRESS TEST VIL	3	16	TP3		0.0		0.4
6-6	682	2AA	1252	ADDRESS TEST VIH	3	15	TP3		1.3		1.9
6-7	682	2AA	1252	ADDRESS TEST VIL	3	14	TP3		0.0		0.4
6-8	682	2AA	1252	ADDRESS TEST VIH	3	13	TP3		1.3		1.9

-Switch S1 must be depressed for accurate readings.
-Analog card JP1 in "B" position.
-Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below.

Adjustments are located on the power supply board. See programmer manual. See NOTE 1.

Confirm programmer in STOP.

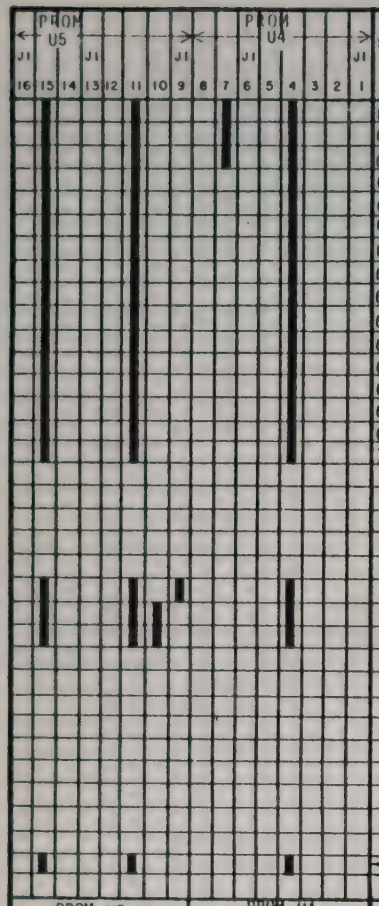
Test point located on analog card.

Momentarily ground TP3; Confirm programmer in STOP.

Load bits 2,4,6,8 ON (Hex AA) to DI bus. Confirm bits 2,4,6,8 ON (Hex 55) on DO bus.

Load bits 1,3,5,7 ON (Hex 55) to DI bus. Confirm bits 1,3,5,7 ON (Hex AA) on DO bus.

Model 5 only: Load bits 1,3,5, and 7 to DI bus. All programmers: confirm all bits OFF (Hex FF) on DO bus.



CALIBRATION CHART 017-1416-1 (CONTINUED)
PAGE 2 OF 7

STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	TEST DESCRIPTION	SWITCH POSITIONS S2	S3	MEASUREMENT PRESS S1 TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
6-9	682	2AA	1252	ADDRESS TEST VIL	3	2	TP3		0.0		0.4	
6-10	682	2AA	1252	ADDRESS TEST VIH	3	3	TP3		1.3		1.9	
6-11	682	2AA	1252	ADDRESS TEST VIL	3	4	TP3		0.0		0.4	
6-12	1365	555	2525	ADDRESS TEST VIH	3	20	TP3		1.3		1.9	
6-13	1365	555	2525	ADDRESS TEST VIL	3	19	TP3		0.0		0.4	
6-14	1365	555	2525	ADDRESS TEST VIH	3	18	TP3		1.3		1.9	
6-15	1365	555	2525	ADDRESS TEST VIL	3	17	TP3		0.0		0.4	
6-16	1365	555	2525	ADDRESS TEST VIH	3	16	TP3		1.3		1.9	
6-17	1365	555	2525	ADDRESS TEST VIL	3	15	TP3		0.0		0.4	
6-18	1365	555	2525	ADDRESS TEST VIH	3	14	TP3		1.3		1.9	
6-19	1365	555	2525	ADDRESS TEST VIL	3	13	TP3		0.0		0.4	
6-20	1365	555	2525	ADDRESS TEST VIH	3	2	TP3		1.3		1.9	
6-21	1365	555	2525	ADDRESS TEST VIL	3	3	TP3		0.0		0.4	
6-22	1365	555	2525	ADDRESS TEST VIH	3	4	TP3		1.3		1.9	
6-23	1365	555	2525	ADDRESS TEST VIH (STOP)	7	4	TP3		1.5		2.5	Set programmer in STOP.
7-1	1365	555	2525	GROUND TEST	8	24	TP3		0.0		0.08	
				PERFORM INTERACTIVE TESTS								
8-1	028	1C	034	ABORT TEST								
8-2	029	1D	035	INTERACTIVE TEST								
8-3	030	1E	036	INTERACTIVE TEST								
				←DATA PATTERN FOR ALL WORDS NOT SHOWN								

FOR DETAILED INSTRUCTIONS REFER TO INTERACTIVE TESTS, NEXT PAGE

PROM U5 TRUTH TABLE
LINE = HI (1), NO LINE = LOW (0)

WORD	04	03	02	01
0-47				
48-49				
50				
51-63				
64-79				

PROM U4 TRUTH TABLE

WORD	04	03	02	01
80				
81-84				
85				
86				
87-127				
128-255				

PROM U3 TRUTH TABLE

NOTES:
1. For the System 19, the limits for this test are 0.1 volt less than specified.
2. JP1 AND 2 ON CAL. ADAPTER TO POSITION B FOR INTERACTIVE TEST ONLY.

NOTES FOR

MODEL IX CALIBRATION

WITH EXISTING SOFTWARE

Note A:

To verify Stop condition, press PROM key, observe output display, should be blank. To resume testing, press Keyboard, then Execute.

Note B:

To observe output buss LED display, press PROM key.

Note C:

To perform "Programmer in FWD," "Programmer in REV" tests, do the following:

a. Ground J1-16 on Analog card
b. Select Load, Execute
c. Press Keyboard, load Hex data 01 for Address 1 only
d. Select Verify, Execute
e. Perform all tests specifying Programmer in FWD
f. Press Skip
g. Perform all tests specifying Programmer in REV
h. To repeat test, select Verify, Execute
i. Remove J1-16 jumper
j. Press Stop, Keyboard, Execute

Note D:

To perform test, press Keyboard; this will pull Stop. To resume testing, press Execute.

Note E:

To perform test:

Clear RAM: Select Invert, press Edit and hold while pressing Load.

a. Press Keyboard, set Address to 000. Load Hex data pattern as called out on calibration chart.
b. Select Program.
c. Ground J1-16 on Analog card
d. Press Execute, wait for programmer to abort; Stop, Keyboard, Execute
e. Release Ground on J1-16
f. Advance to word count specified on calibration chart to make measurement
g. Press PROM for output display, perform measurement
h. Repeat steps a-g for compliment data pattern

Certain MOS Program Card Sets utilize interactive programming techniques. That is, pulse duty cycles are controlled by PROM temperature, and the re-program pulse train lengths are proportional to the number of pulses required to initially program particular PROM words.

Performance check of MOS interactive functions requires installation of the Digital Card into the Universal Calibrator. These tests, if required, are found at the bottom of the Calibration Chart under the heading, "INTERACTIVE PROGRAMMING TESTS," and should be performed following Analog Card tests.

1. Turn programmer power OFF.
2. Unplug connector J1 and connector J2 at the Universal Calibrator.
3. Connect J1 Pin 3 of Digital Card to J1 Pin 3 of Calibrator (CAUTION: do not use 16 pin cable).
4. With Calibration Adapter assemblies 702-1073 Rev. "E" or later, install JP1 and JP2 in Pos. "B".

Test Procedure:

To test the interactive programming functions of the MOS Digital Card, proceed as follows:

1. Initialization

   a. Turn Programmer power ON.
   b. Press Keyboard.
   c. Set Address 01C.
   d. Load Data 01.

2. Abort Test

   * a. Press Program (Press Execute)
   * b. Press Execute (Hold SET key depressed and press FWD key)
   c. After several seconds, observe PASS indicator, with Programmer word count at 01C, and P light blinking.

3. Interactive Tests

   a. Press Stop
   b. Press Keyboard
   c. Load data 00 on word count 01C.
   d. Advance word count to 1D by pressing FWD.
   e. Load Data 01.
   * f. Press Program (Press Execute)
   * g. Press Execute (Hold SET key depressed and press FWD key)
   * h. After several seconds, observe PASS indicator with programmer word count at 01D and V lights blinking. (01E)

This completes test procedures for MOS Digital Cards with interactive programming capabilities. If FAIL is indicated in any of the above test, DO NOT use the Digital Card for PROM programming.

* For programmers using software 010-5900 Rev. C or later, data in parentheses replaces underlined data.

MOS INTERACTIVE PROGRAMMING TESTS FOR P5

Certain MOS Program Card Sets utilize interactive programming techniques. That is, pulse duty cycles are controlled by PROM temperature, and the re-program pulse train lengths are proportional to the number of pulses required to initially program particular PROM words.

Performance check of MOS interactive functions requires installation of the Digital Card into the Universal Calibrator. These tests, if required, are found at the bottom of the Calibration Chart under the heading "INTERACTIVE PROGRAMMING TESTS," and should be performed following Analog Card tests.

1. Turn Programmer power OFF.

2. Unplug connector J1 and connector J2 at the Universal Calibrator.

3. Remove Analog Card with attached 26-conductor and 16-conductor cables and set aside.

4. Install calibrator into Digital Card slot.

5. Insert Digital Card (components forward) into Universal Calibrator top edge connector.

6. Connect J1 Pin 3 of Digital Card to J1 Pin 3 of Calibrator. CAUTION: do not use 16 pin cable.

7. With Calibration Adaptors using 702-1073 Rev. "E" assemblies or later, install JP1 and JP2 in Position B.

Test Procedure: To test the interactive programming functions of the MOS Digital Card, proceed as follows:

1. Initialization

   a. Turn Programmer power ON.

   b. Press: RESET
      MANUAL
      ROM 2 - ROM 2
      PROGRAM
      START

2. Abort Test

   a. Slew Programmer Word Count FWD to:

DEC	HEX	OCT
28	1C	034

   b. STOP

   c. START

   d. Load input Bit 1 (only)

   e. FWD (momentarily)

   f. After several seconds, observe PASS/FAIL indicator; if PASS is indicated Data A and Data B lights should be extinguished.

3. Interactive tests

   a. STOP

   b. START

   c. FWD to Word Count

DEC	HEX	OCT
29	1D	035

   d. Load input Bit 1 (only)

   e. FWD (momentarily)

   f. Observe PASS/FAIL indicators, with Programmer Word Count at:

DEC	HEX	OCT
30	1E	36

This completes test procedures for certain MOS Digital Cards with interactive programming capabilities. If FAIL is indicated in any of the above tests, DO NOT use the Digital Card for PROM programming.

CIRCUIT DESCRIPTION

CIRCUIT DESCRIPTION, PROGRAM CARD SET

INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 4-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signaled, or until the bit is programmed.

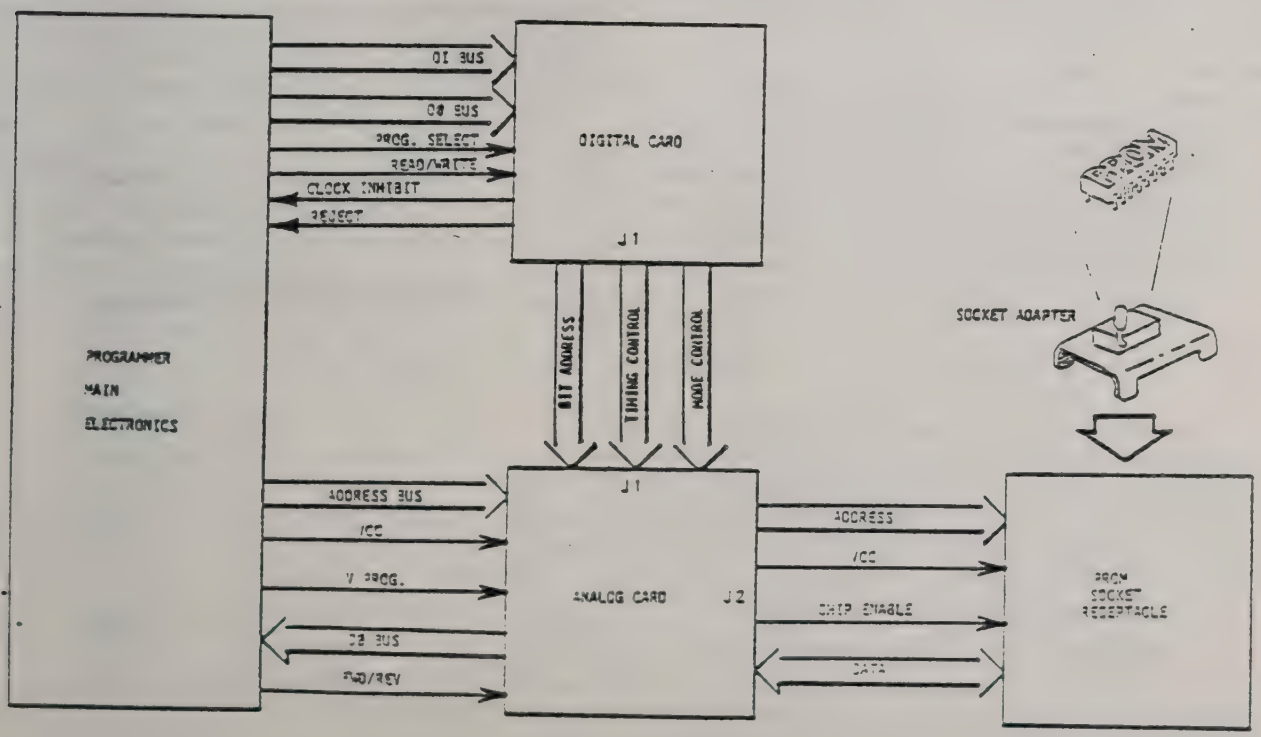
ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturer's specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow and timing. ROM truth tables, timing diagrams, jumper positions, and reject conditions are discussed. Detailed circuit schematics with timing diagrams and truth tables are found at the rear of this manual--refer to these for pin-out and interconnect information.

Fig. 4-1. Simplified Block Diagram of Program Card Set



DIGITAL CARD CIRCUIT DESCRIPTION

The digital card block diagram is shown in Figure 4-2. The digital card receives control signals from the programmer bus shown in the diagram on the left side and outputs control signals to the analog card on the right.

TWO SPEED CLOCK

The TWO SPEED CLOCK is the master clock for the card set and is used to time the operation of the sequence counters, sequence register, and pulse counters. The sequence PROM controls the clock speed via the sequence register.

SELECT LOGIC

The SELECT LOGIC is the interface between the program card set and the programmer, coordinating control between them.

The PROG, WRITE, WRITE INHIBIT, READ INHIBIT, and READ inputs select and initiate the functions of the digital card. The VFY A, and VFY B outputs tell the programmer whether to verify 4 or 8 bits. Both go high to signal an abort condition to the programmer if the PROM fails to program.

The BUSY output is pulled low by the digital card during the programming sequence for a given word. Once the word is programmed, BUSY goes high and the programmer verifies the programmed data and continues to the next word. If a word fails to program, the digital card will stop with VFY A and VFY B high and BUSY low, locking the programmer on that word address.

The Q output of the select memory is labelled INITIALIZE on the block diagram. When the card set is not selected, this line is low, clearing the BTP MEMORY SEQUENCE counter and PROG counters. The OVERPROGRAM counter is preset according to JP1 by the $\overline{Q}$ side of the SELECT memory.

BIT COMPARE GATES

The BIT COMPARE GATES determine whether the card set needs to go into PROGRAM for a given word. The gates accomplish this by comparing the states of the DI bus (RAM DATA) and the DO bus (PROM DATA). Whether 4 or 8 bits are compared is controlled by the $\overline{4}/8$ line from the socket adapter. The output from these gates sets the BIT-TO-PROG memory which starts the program algorithm and controls the UP/DOWN inputs of the PROGRAM PULSE counters for the purpose of interactive program control. (Refer to the "PULSE COUNTERS" paragraph.)

BIT-TO-PROGRAM MEMORIES

The BIT–TO–PROGRAM MEMORIES control entry into and looping through the program waveforms. When the BIT COMPARE GATES determine there are bits to be programmed, this memory will cause programming to continue until the pulse counters have counted back to zero. The NO-BTP MEMORY gets set if the BTP MEMORY is not set. This memory will terminate the operation of the card for the present word address since the PROM data already matches the RAM data.

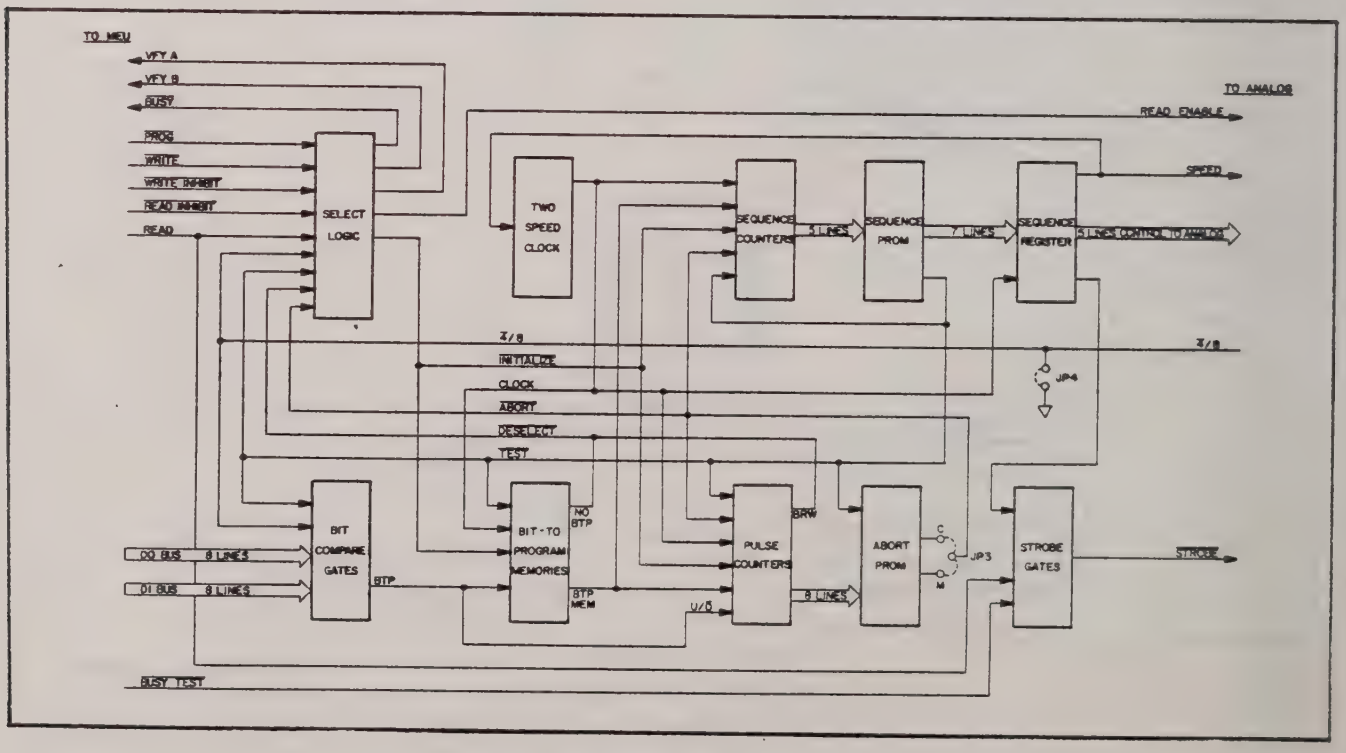


Figure 4-2. Block Diagram, 701-1446 Digital Card.

THE SEQUENCE COUNTER AND SEQUENCE PROM

The SEQUENCE COUNTERS count through the addresses of the SEQUENCE PROM to generate the programming waveform timing. The sequence PROM also outputs a TEST pulse which is used as an enable for the SELECT LOGIC, BIT COMPARE GATES, BIT-TO-PROG MEMORIES, PULSE COUNTERS, ABORT PROM, and SEQUENCE COUNTERS.

SEQUENCE REGISTER

The SEQUENCE REGISTER is used to remove the decoding glitches from the outputs of the sequence PROM. The outputs of the register are the control signals to the analog card.

STROBE GATES

The STROBE GATES generate a strobe to the analog card while U1-12 is low, and also for approximately 4 μs at the leading edge of a high-going READ, or low-going BUSY TEST. This STROBE latches address and updates data in the PROM being programmed.

PULSE COUNTERS

An 8 bit PROGRAM COUNTER and a 4 bit OVER-PROGRAM COUNTER count program and overprogram pulses. While the bits still test unprogrammed, the 8 bit PROGRAM COUNTER increments for each PROGRAM pulse. After the bits have programmed, this counter begins to decrement but is enabled only during the borrow from the OVER-PROGRAM COUNTER. The OVER-PROGRAM counter decrements to zero from the JP1 preset valve. At zero, the borrow enables the PROGRAM COUNTER to count down and also causes the OVER-PROGRAM COUNTER to preset back to the JP1 value. When the PROGRAM COUNTER reaches zero, its borrow output resets the SELECT memory, terminating the operation of the card set for this word address.

The total number of pulses to the PROM is shown by the following equation:

$n = x + x(A + 1)$ where n = total pulses

x = initial pulses

A = binary value of JP1

By this equation, if it takes 4 pulses to program and JP1 is set for 3, then a total of 20 pulses will be applied to the PROM.

ABORT PROM

The ABORT PROM causes the card set to stop in an ABORT condition after the PULSE COUNTERS have counted up to the abort limit. This limit is selected by JP3 at either of two preset values between 1 and 255 pulses. Refer to the timing diagram for the JP3 values.

ANALOG CARD CIRCUIT DESCRIPTION

BLOCK DIAGRAM

Figure 4-3 gives a generalized block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) at the rear of this manual for details of circuit connection and operation.

The following paragraphs discuss the functions contained on the analog card.

Address buffers accommodate the ten incoming address lines emanating from the programmer MEU. The buffers consist of non-inverting gates with uncommitted collector outputs. Buffer outputs have resistor pull-ups to PROM Vcc.

VCC GENERATOR

The Vcc generator consists of a common emitter amplifier (Q7) controlled by a differential amplifier (Q3 and Q4). R11 provides a feedback path to the amplifier and serves as output voltage adjustment. The reference for the differential amplifier is determined by adjustable shunt regulator (Q6) and voltage divider action of R9, R14, and R15.

The generator output is held to zero volts when the programmer is in Stop. Fold back current limiting is accomplished via Q5, Q8, and Q20. When excess Vcc current is drawn, Q8 turns on, turning on Q5 and Q20. Q5 holds the shunt regulator output (differential reference) to 0 volts, thereby holding Vcc to 0 volts. Q20 pulls Reset, Reset pulls Stop, and Stop holds the reference to 0 volts.

PROGRAM VOLTAGE GENERATOR

The Program Voltage Generator consists of transistors Q11 and Q12 driven by Q9 and Q10 controlled by the differential amplifier Q13 and Q14. The output is push-pull with active pull up and pull down. The pull up transistor is tied to either + Program or +48 by jumper JP3. The pull down transistor is tied to either -48 generator, -9v, or ground by jumper JP4.

The reference voltage for the differential amplifier is Vcc. R34 provides the negative feedback path. The output voltage is adjusted by R3 or R4. R3 and R4 are jumpered to J1-5 and J1-6 by JP1 and JP2, or are switched to the shunt regulator (Q6) output by Q1 and Q2. When J1-5 and J1-6 are high, the generator output sets at the

value of Vcc. When J1-5 or J1-6 are low, the output can be adjusted below Vcc and to a negative value. Fold back current limiting is present on both the pull up and pull down source. The output is held to 0 volts when the programmer is in Stop.

NEGATIVE VOLTAGE GENERATOR

This generator, a modified voltage doubler is used to generate a negative voltage source. Oscillator U9, transistors Q17-19, provide a 48 volt square wave pulse. Capacitors C6, C7 and diodes CR3, CR4 shift polarity of the 48 volt pulse, providing a -48V dc source.

DATA BUS DRIVERS

Data from the DI Bus is presented to Gates U2, U3, U6 and U7. Outputs from these gates drive the PROM bits during program. During Read, Data Enable disables the gate outputs and data from the PROM is presented to the comparator.

COMPARATOR AND DATA OUT DRIVERS

The comparator compares PROM bit data against the reference level. The reference for the comparator is determined by voltage divider R16 and R17. Comparator outputs are transferred to the DO Bus during Read by the data out drivers. This transfer allows the digital card to make a digital comparison of the transferred PROM output (DO Bus) to the programmer DI Bus.

CHIP ENABLE AND OD BUFFERS

These buffers output the specified CE and OD voltage levels to the PROM during Program and Read. Their outputs are resistively pulled up to the Vcc supply.

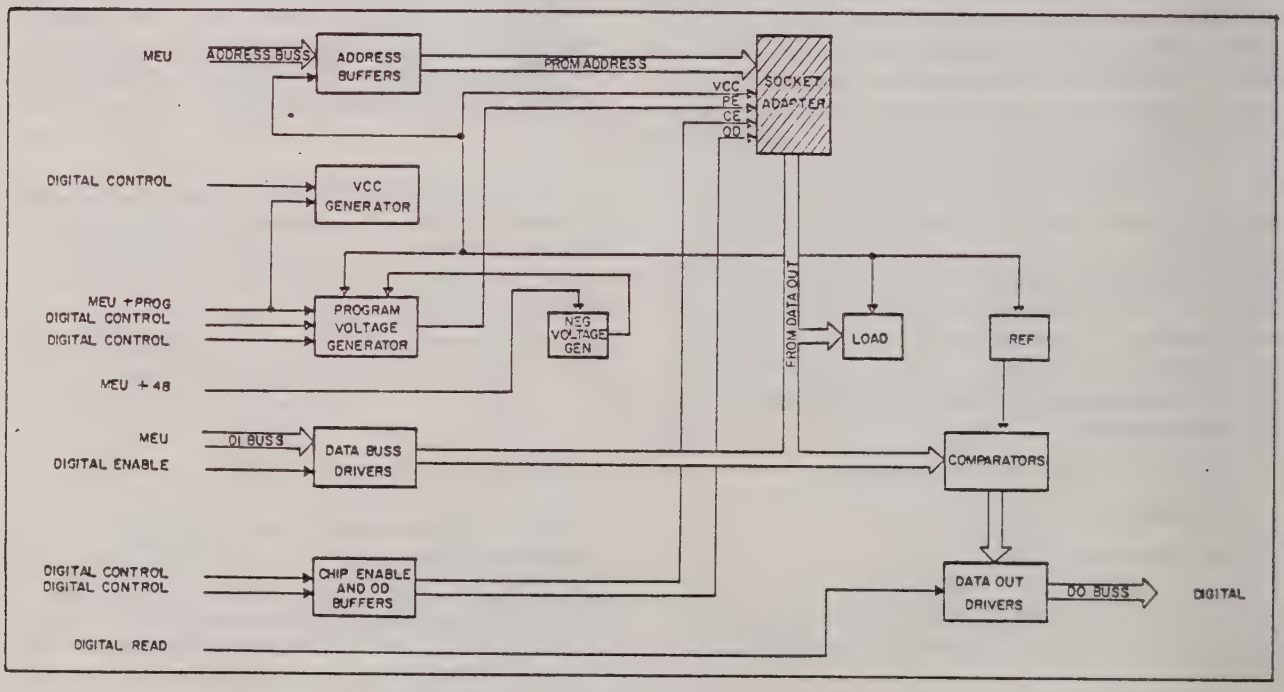


Figure 4-3. Block Diagram, 701-1446 Analog Card

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

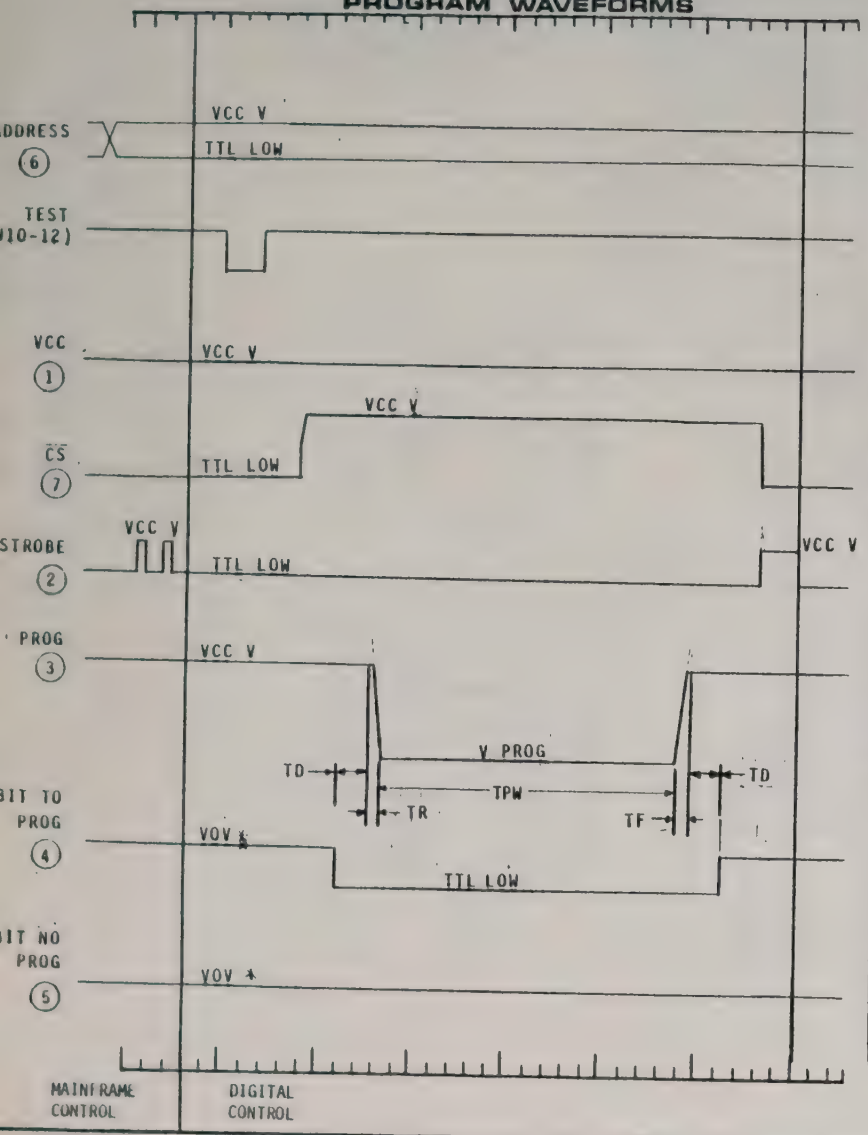
Please send all parts orders to:

DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

PROGRAM WAVEFORMS



NOTES

701-1446 JUMPERS

JP1	A,B	OPEN
	C,D	SHORT
JP2		SHORT
JP3	C=2	PULSE REJECT
	M=1	PULSE REJECT
JP4		OPEN

WAVEFORM VARIABLES

VCC V	=	5 ± 0.25V
VOV	=	2.5 ± 0.4V
VOP	=	5.0 ± 0.7V
V PROG	=	-44 ± 2V
TTL LOW	=	0.0 - 0.4V
TD	=	10us min
TPW	=	20 ± 3ms
TR, TF	=	2-10us

V PROG DUTY CYCLE 80% MAX.

* DUE TO CALIBRATION TEST LOADS, THESE VOLTAGES ARE APPROXIMATELY HALF THEIR NORMAL PROGRAMMING LEVELS.

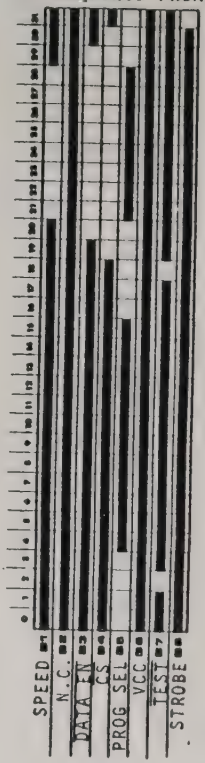
○ THESE WAVEFORMS CORRESPOND TO CALLOUTS ON THE CALIBRATION CHART. SWITCH S2 AND S3 OF THE UNIVERSAL CALIBRATOR TO INDICATED POSITIONS, TO OBTAIN WAVEFORMS. REFER TO PERFORMANCE CHECK SECTION OF MANUAL FOR DETAILED STEPS.

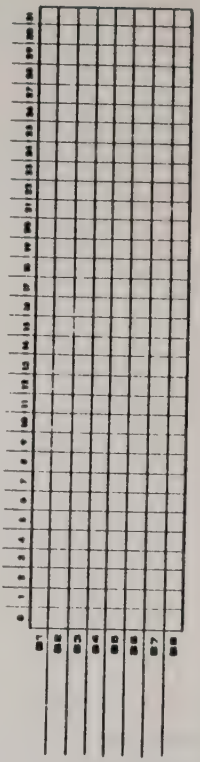
DATE	SYM	REVISION RECORD	DR	CK
3-7-79	A	RELEASE	RK	
7/79	B	ECN#2445	KJ	JSC
1/79	C	ECN #2749	ML	MD

TRUTH TABLES

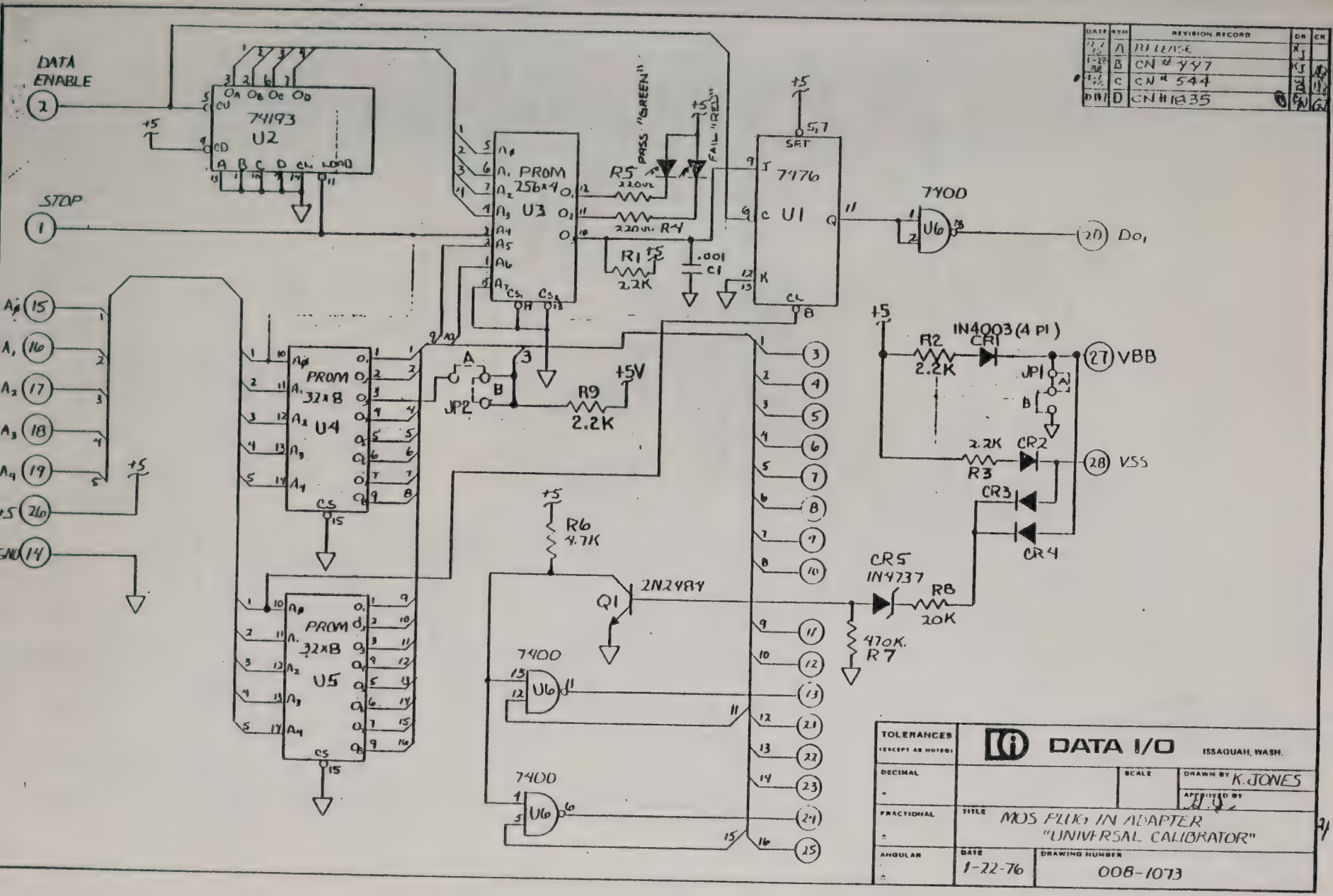
LINE : HI(1); NO LINE : LOW(Ø)

U5 SEQUENCE PROM

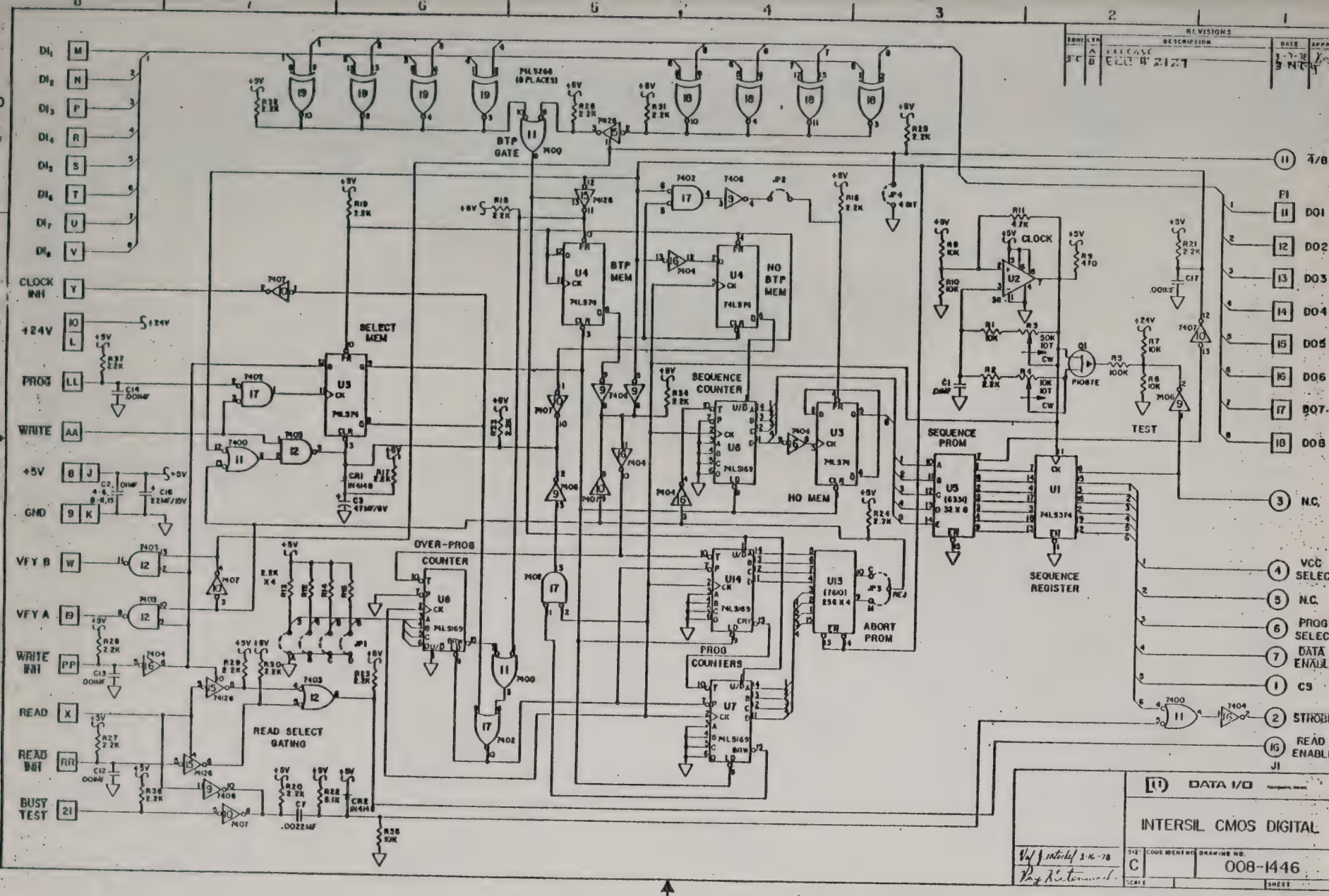


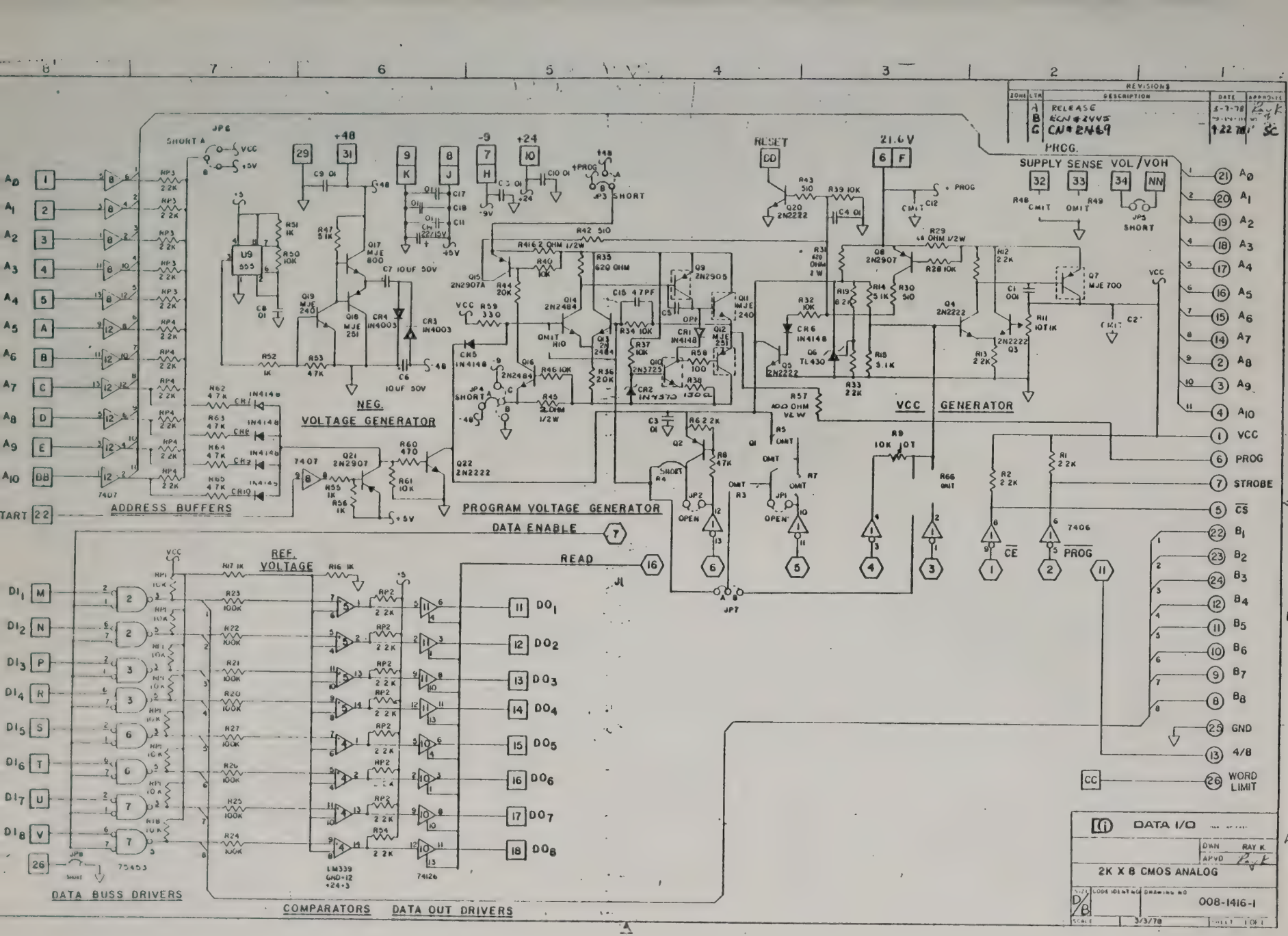


DATA I/O ISSAQUAH, WASH.		
	DRAWN BY	WALTER
	APPROVED BY	Ray K
TITLE	INTERSIL CMOS	
DATE 2-28-78	DRAWING NUMBER	007-1416-1



DATE	SYM	REVISION RECORD	DR	CK
	A	RELEASE		
	B	CN # 497		
	C	CN # 544		
	D	CN # 635		


DI1 M
DI2 N
DI3 F
DI4 R
DI5 S
DI6 T
DI7 U
DI8 V
CLOCK INH Y
+24V 10 L
PROG LL
WRITE AA
+5V B J
GND 9 K
VFY B W
VFY A 19
WRITE INH PP
READ X
READ INH RR
BUSY TEST 21
74LS266 (8 PLACES)
BTP GATE
BTP MEM
NO BTP MEM
SELECT MEM
SEQUENCE COUNTER
HO MEM
SEQUENCE PROM
SEQUENCE REGISTER
CLOCK
PROG
TEST
OVER-PROG COUNTER
PROG COUNTERS
ABORT PROM
READ SELECT GATING
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
N.C.
VCC SELEC
N.C.
PROG SELEC
DATA ENABL
C9
STROBE
READ ENABL
DATA I/O
INTERSIL CMOS DIGITAL
008-1446


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A RELEASE 5-7-78
B ECN #2445
C CN# 2469
PROG.
SUPPLY SENSE VOL/VOH
RESET
21.6V
NEG. VOLTAGE GENERATOR
VCC GENERATOR
PROGRAM VOLTAGE GENERATOR
ADDRESS BUFFERS
DATA ENABLE
READ
REF. VOLTAGE
DATA BUSS DRIVERS
COMPARATORS
DATA OUT DRIVERS
DATA I/O
2K X 8 CMOS ANALOG
008-1416-1
DWN RAY K.
APVD
3/3/78

90 Day Warranty

Data I/O warrants that all equipment sold pursuant to any resultant agreement shall be free from defects in material or workmanship at the time of delivery. Such warranty shall extend for 90 days. Buyer must provide notice to Data I/O within this prescribed warranty period of any defect; if the defect is not the result of improper usage, service, maintenance or installation and equipment has not been otherwise damaged or modified after delivery, Data I/O shall either replace or repair the defective part or parts of equipment or replace the equipment or refund the purchase price at Data I/O's option after return of such equipment by buyer to Data I/O. Shipment to and from Data I/O's facility shall be borne on account of buyer.

(a) Consequential Damages — Data I/O shall not be liable for any incidental or consequential damages incurred as a result of any defect in any equipment sold hereunder and Data I/O's liability is specifically limited to its obligation described herein to repair or replace a defective part or parts covered by this warranty.

(b) Exclusive Warranty — The warranty set forth herein is the only warranty, oral or written made by Data I/O and is in lieu of and replaces all other warranties, expressed or implied, including the WARRANTY OF MERCANTIBILITY AND THE WARRANTY OF FITNESS FOR PARTICULAR PURPOSE.

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DATA I/O

Programming systems for tomorrow...today

Reader Comments

The manual's completeness, accuracy, organization, usability, and reliability: _____

_____

Did you find errors in this manual: _____

How can this manual be improved: _____

_____

_____

Additional comments: _____

_____

Name _____

Company _____ Department _____ M/S _____

Address _____

City _____ State _____ Zip _____ Phone _____

Manual or Part No. _____

Warranty/Registration

Please return this card to Data I/O within five days

Did the packaging of this equipment exhibit any outward signs of physical damage? . . . . . YES ○ ○ NO
Did this equipment arrive intact, without loose parts or cable damage? . . . . . YES ○ ○ NO
Did the equipment operate on power-up?. . . . . YES ○ ○ NO
Did you attain adequate system performance? . . . . . YES ○ ○ NO
Were any electrical adjustments required? . . . . . YES ○ ○ NO
If you required assistance, was a local Data I/O representative contacted? . . . . . YES ○ ○ NO

Comments – _____

_____

Name _____ Title _____

Department _____ M/S _____

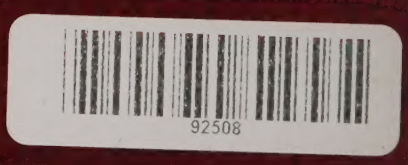
Company _____

Address _____

City _____ State _____ Zip _____ Phone ( ) _____

Model or Description _____ Serial or Part No. _____

Date Received _____



DATA I/O

Programming systems for tomorrow...today